OIPE JC139
JUL 07 2004
PATENT & TRADEMARK OFFICE

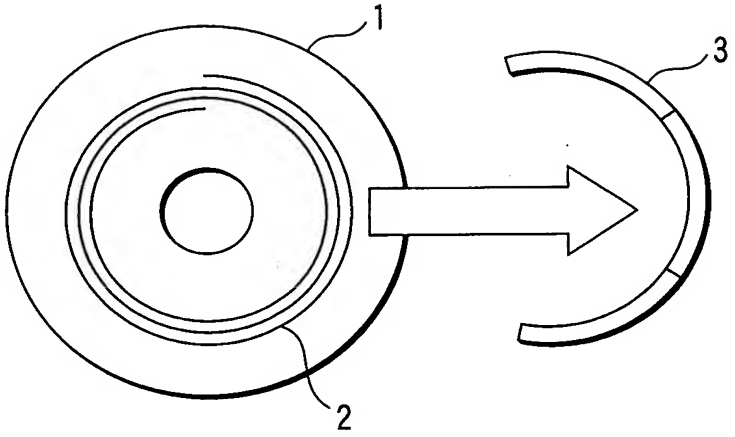


FIG. 1

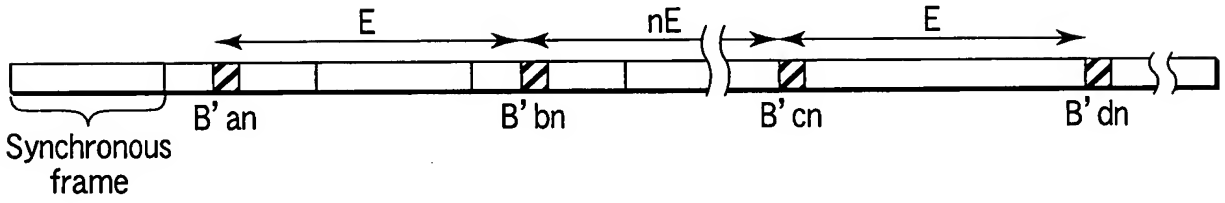


FIG. 3

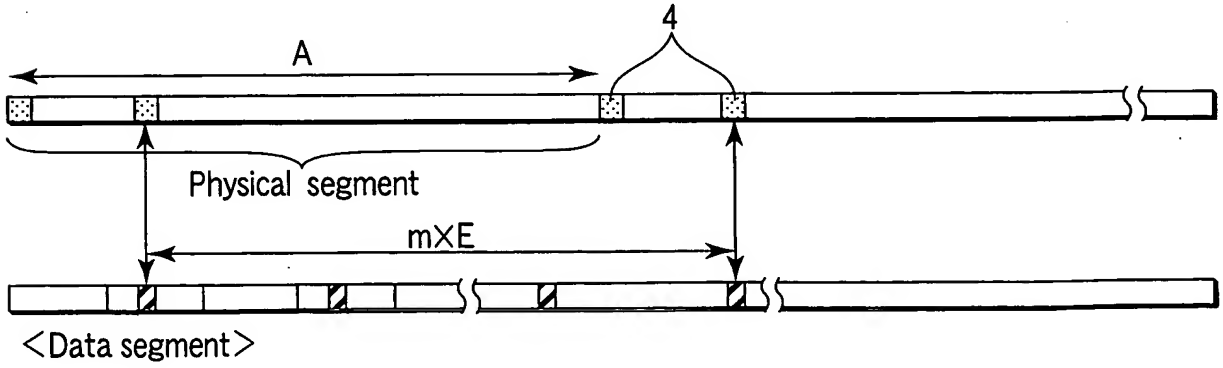


FIG. 4

FIG. 2A

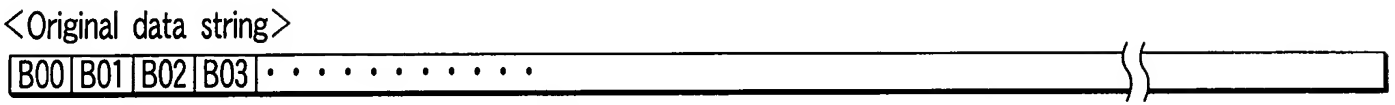


FIG. 2B

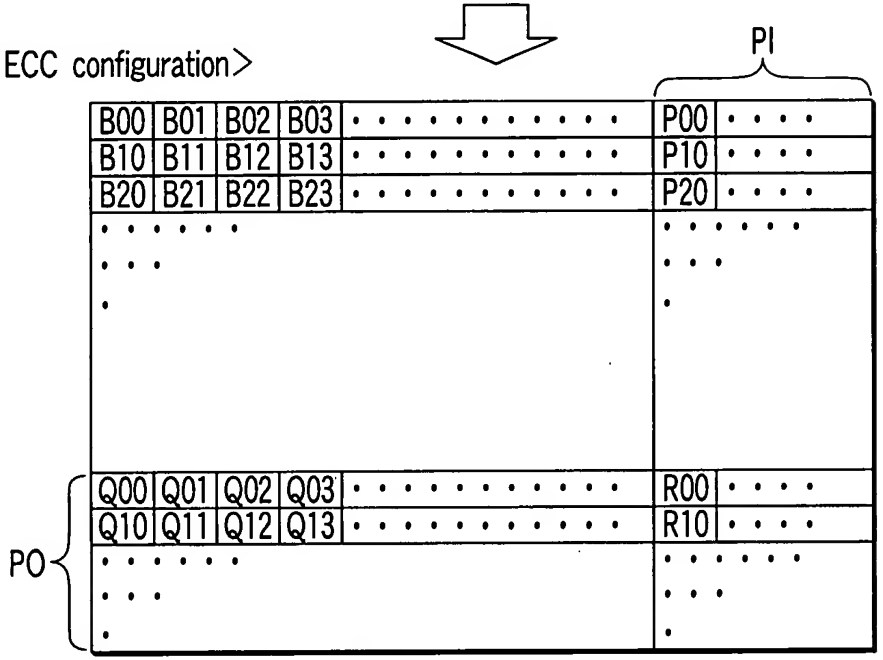


FIG. 2C

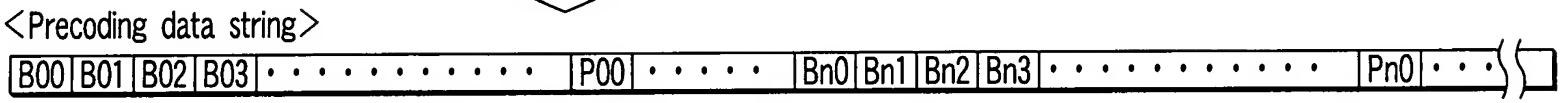


FIG. 2D

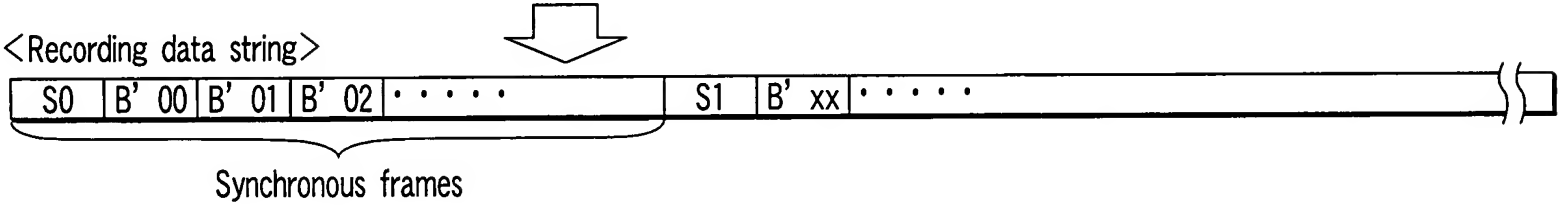


FIG. 5

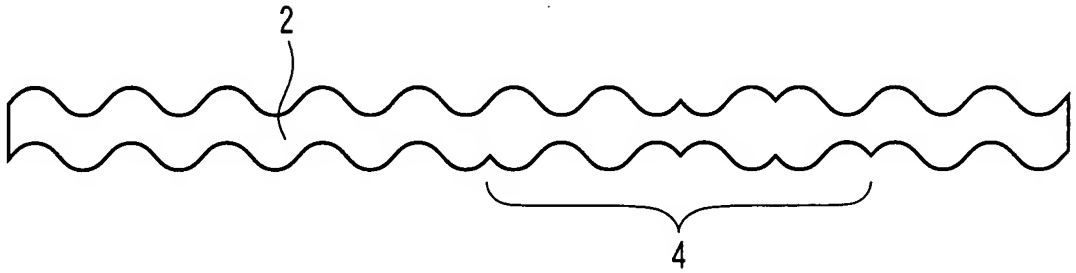


FIG. 6

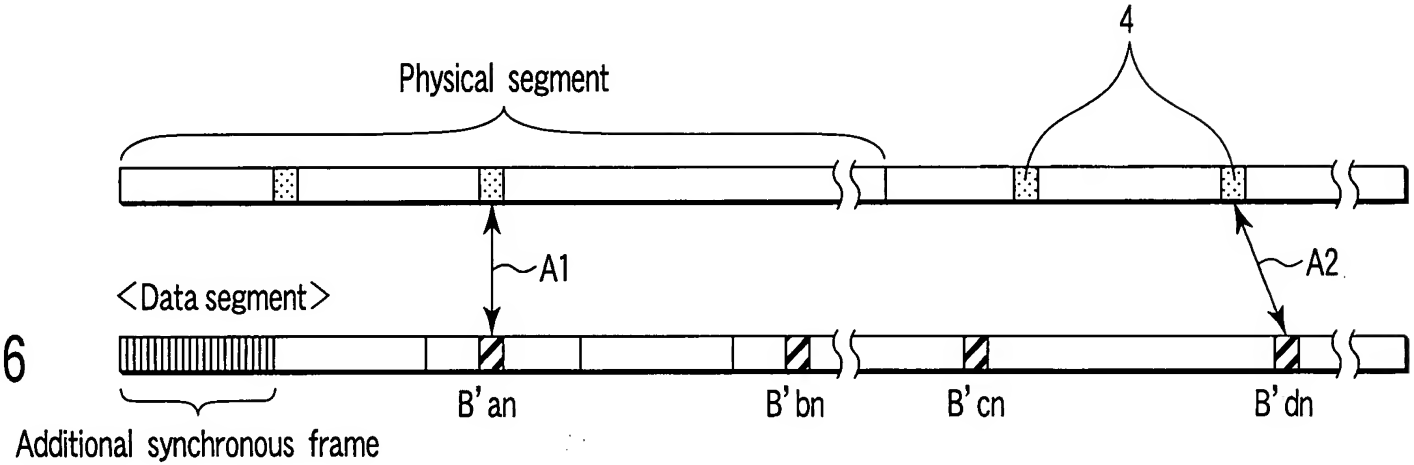


FIG. 7

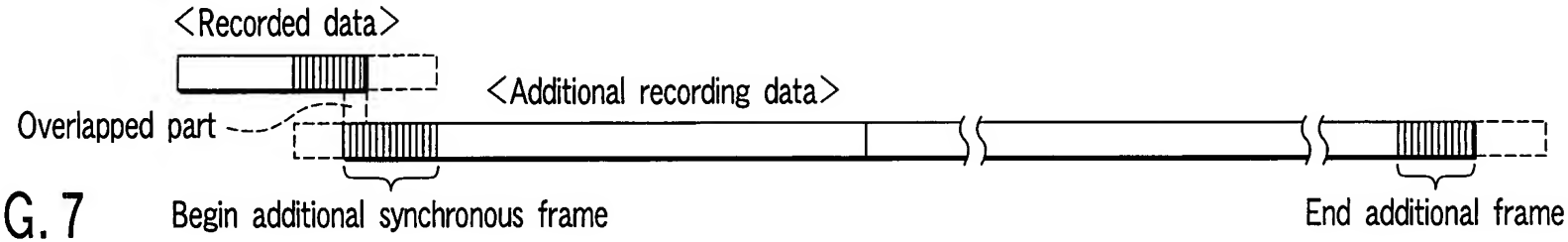


FIG. 8

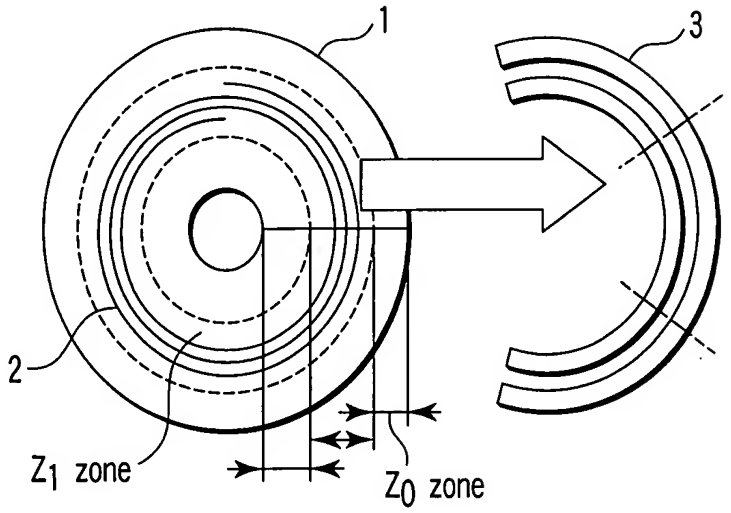
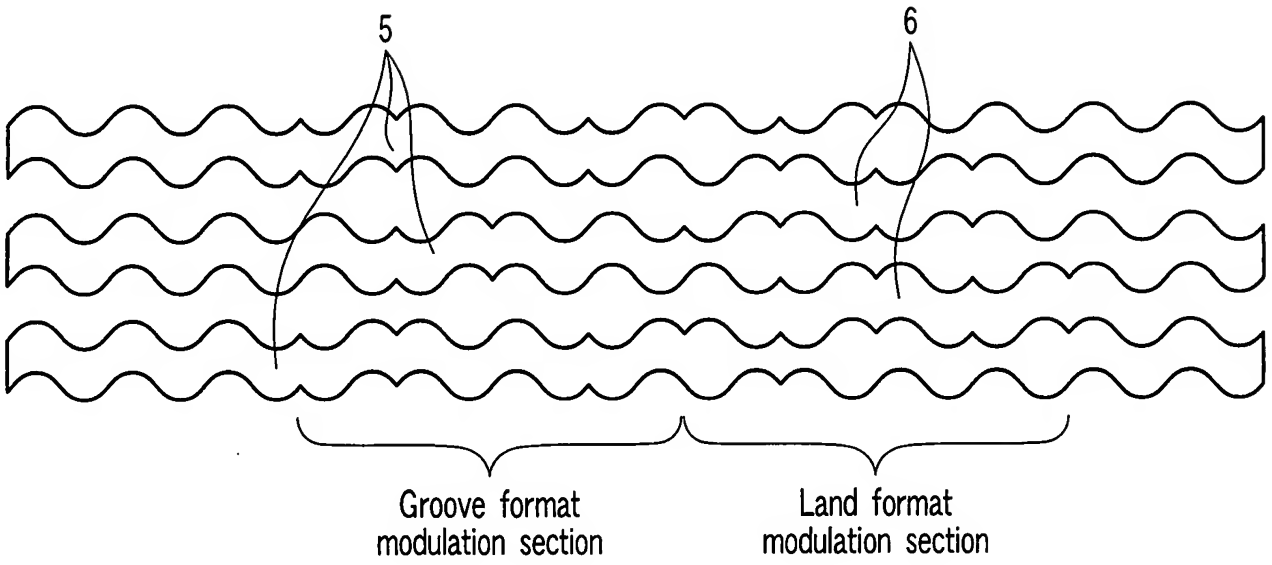

1
3
2
Z_1 zone
Z_0 zone

FIG. 9


5
6
Groove format modulation section
Land format modulation section

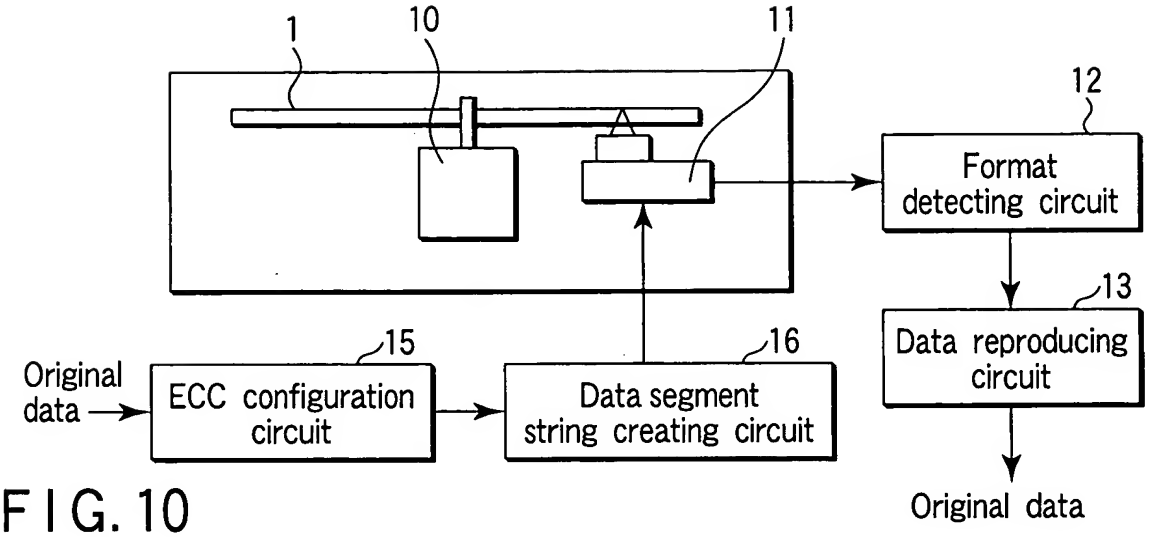


FIG. 10

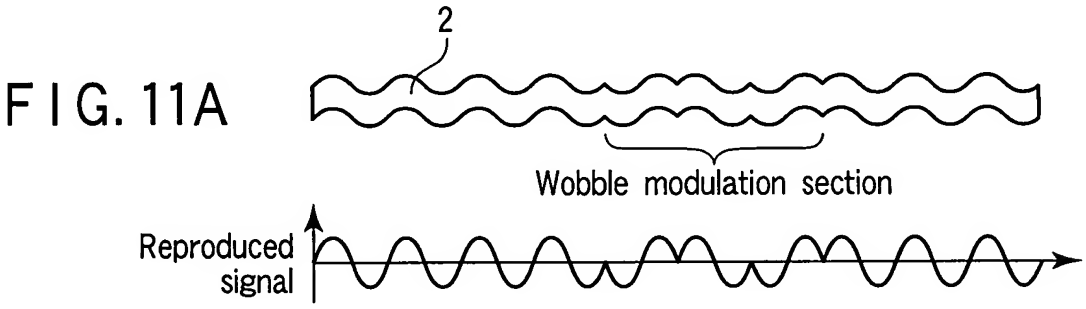


FIG. 11A

FIG. 11B

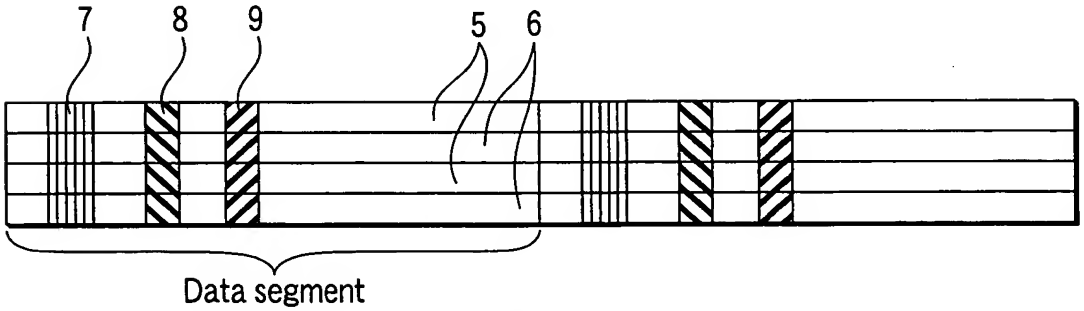


FIG. 12

FIG. 13

Binary code	Gray code
000000	000000
000001	000001
000010	000011
000011	000010
000100	000110
000101	000111
000110	001111

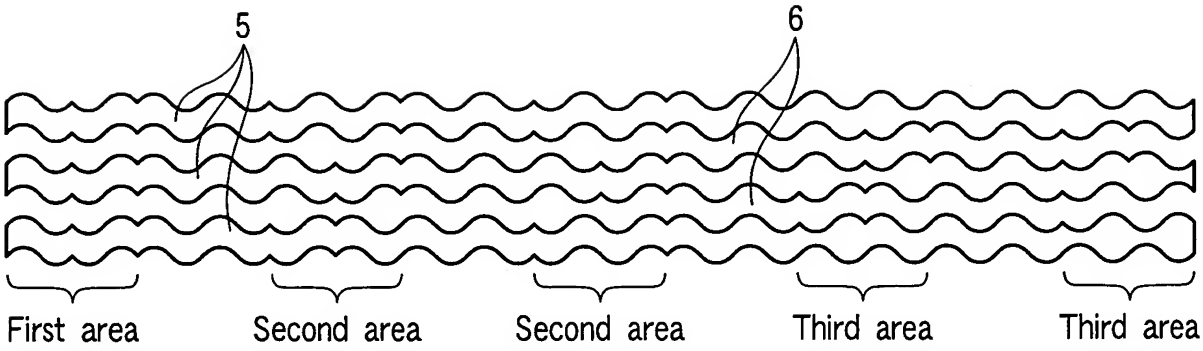


FIG. 14

FIG. 15A

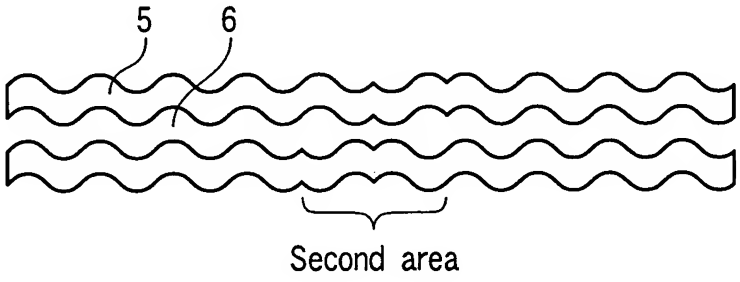


FIG. 15B

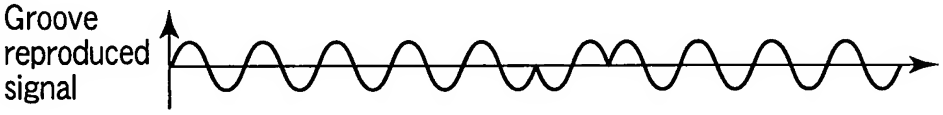
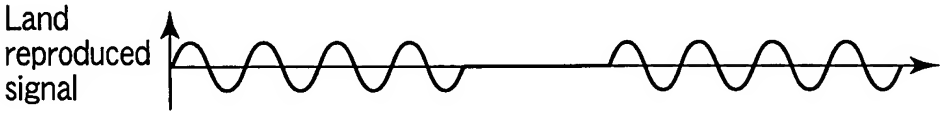


FIG. 15C



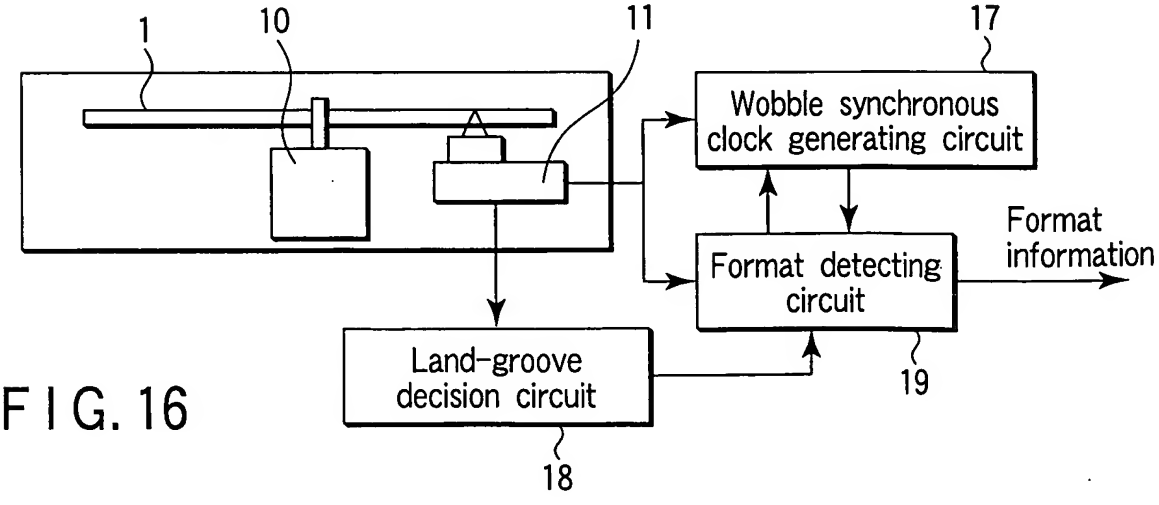


FIG. 16

FIG. 17

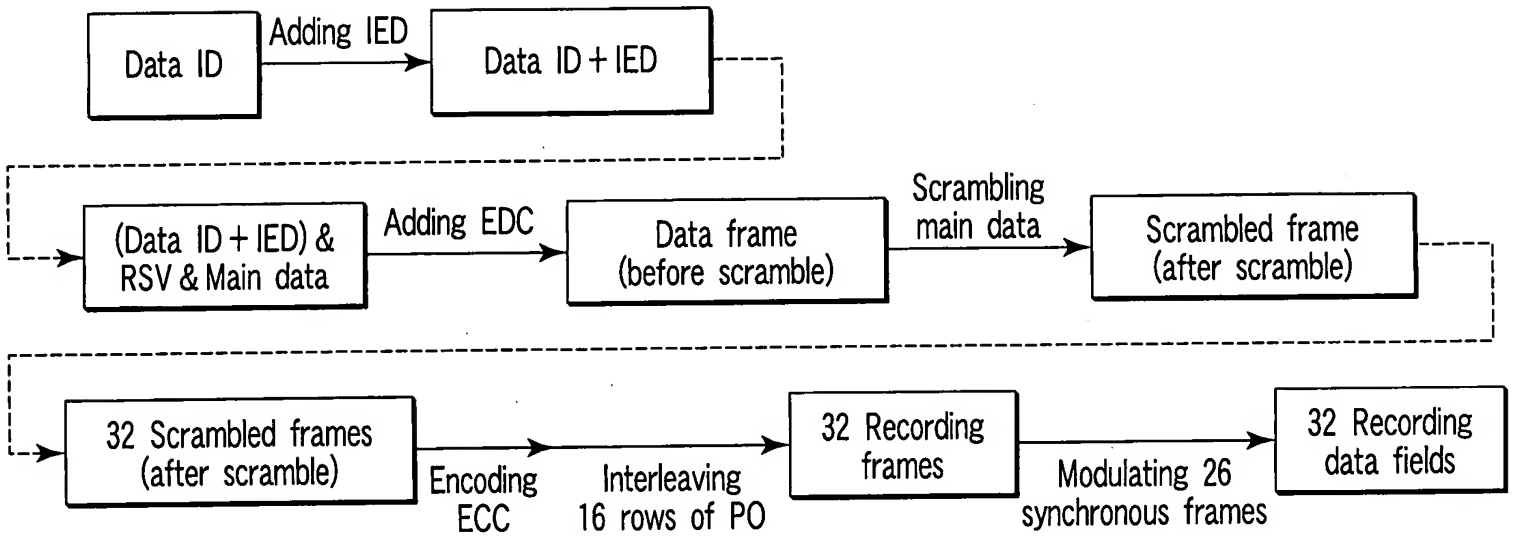

Data ID
Adding IED
Data ID + IED
(Data ID + IED) & RSV & Main data
Adding EDC
Data frame (before scramble)
Scrambling main data
Scrambled frame (after scramble)
32 Scrambled frames (after scramble)
Encoding ECC
Interleaving 16 rows of PO
32 Recording frames
Modulating 26 synchronous frames
32 Recording data fields

FIG. 18

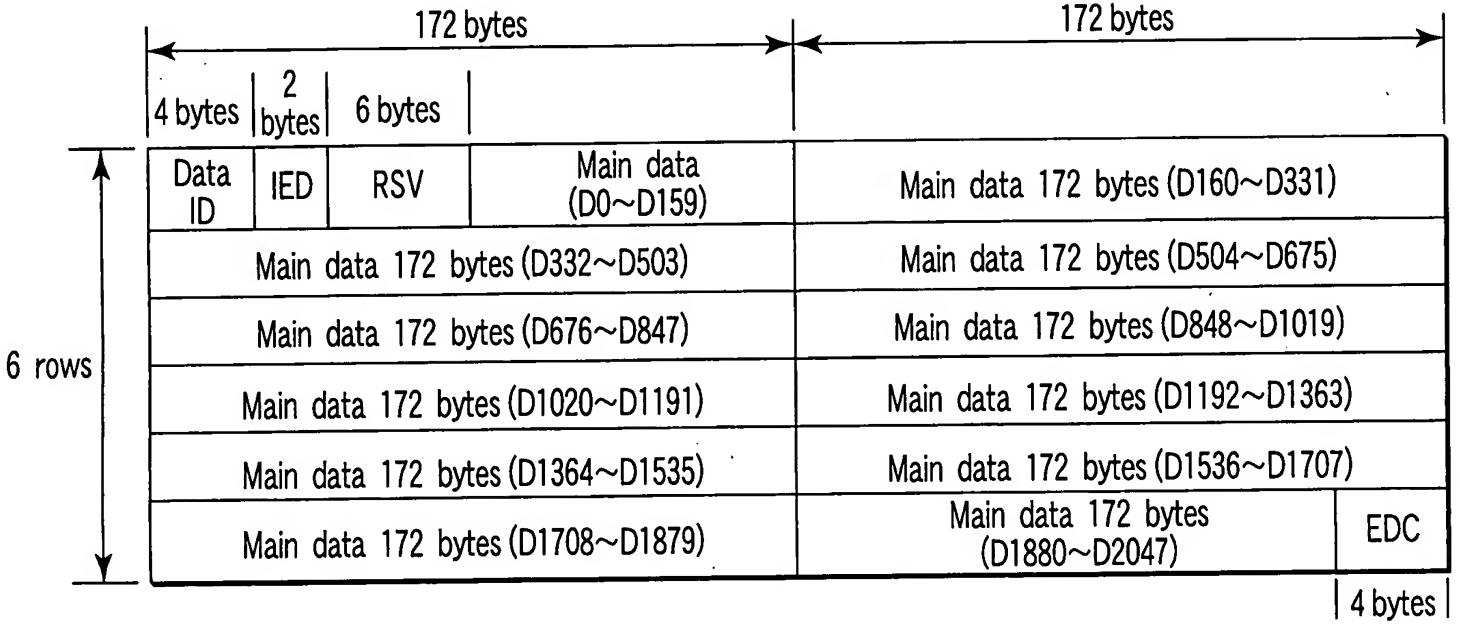

172 bytes
172 bytes
4 bytes
2 bytes
6 bytes
Data ID
IED
RSV
Main data (D0~D159)
Main data 172 bytes (D160~D331)
Main data 172 bytes (D332~D503)
Main data 172 bytes (D504~D675)
Main data 172 bytes (D676~D847)
Main data 172 bytes (D848~D1019)
Main data 172 bytes (D1020~D1191)
Main data 172 bytes (D1192~D1363)
Main data 172 bytes (D1364~D1535)
Main data 172 bytes (D1536~D1707)
Main data 172 bytes (D1708~D1879)
Main data 172 bytes (D1880~D2047)
EDC
6 rows
4 bytes

FIG. 19

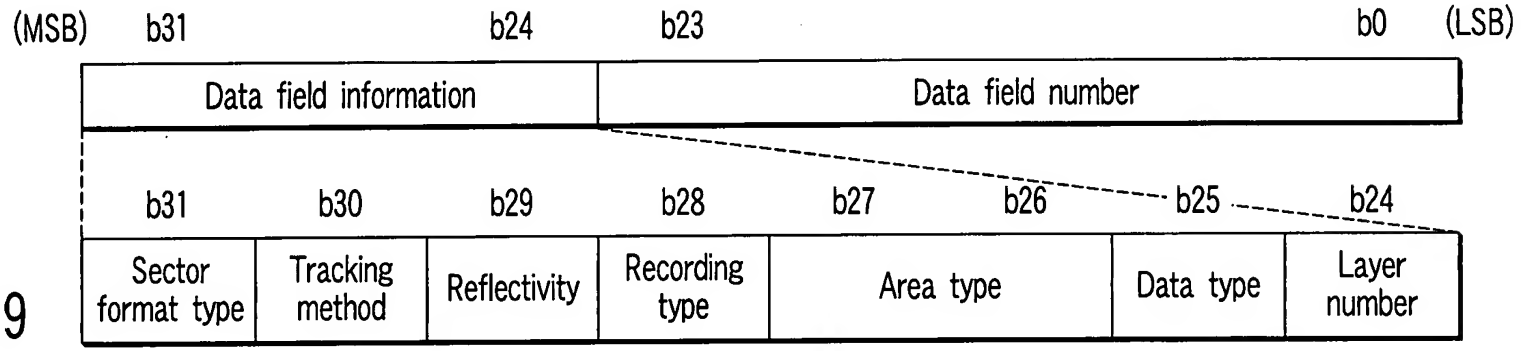
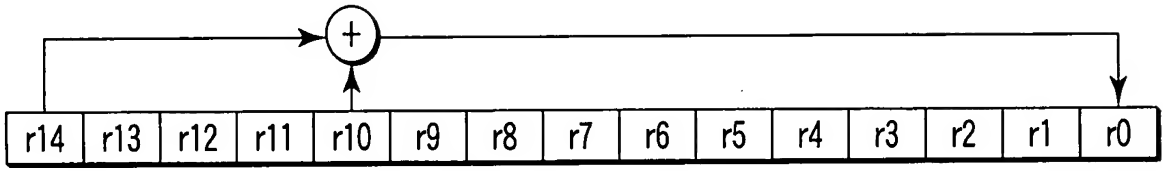


FIG. 20A

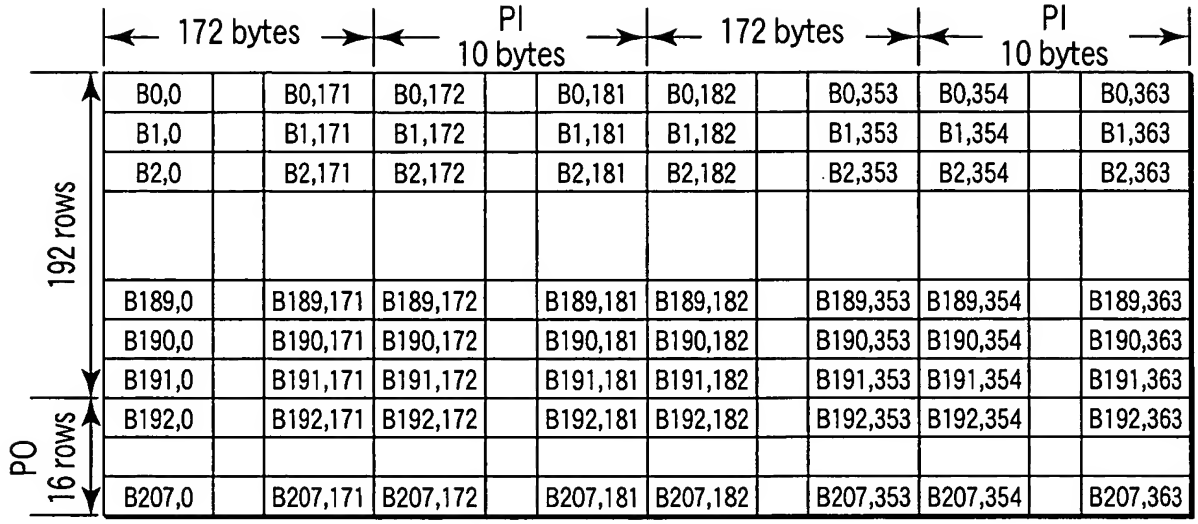
Initial preset number	Initial preset value	Initial preset number	Initial preset value
0h	0001h	8h	0010h
1h	5500h	9h	5000h
2h	0002h	0Ah	0020h
3h	2A00h	0Bh	2001h
4h	0004h	0Ch	0040h
5h	5400h	0Dh	4002h
6h	0008h	0Eh	0080h
7h	2800h	0Fh	0005h

Initial value of shift register

FIG. 20B

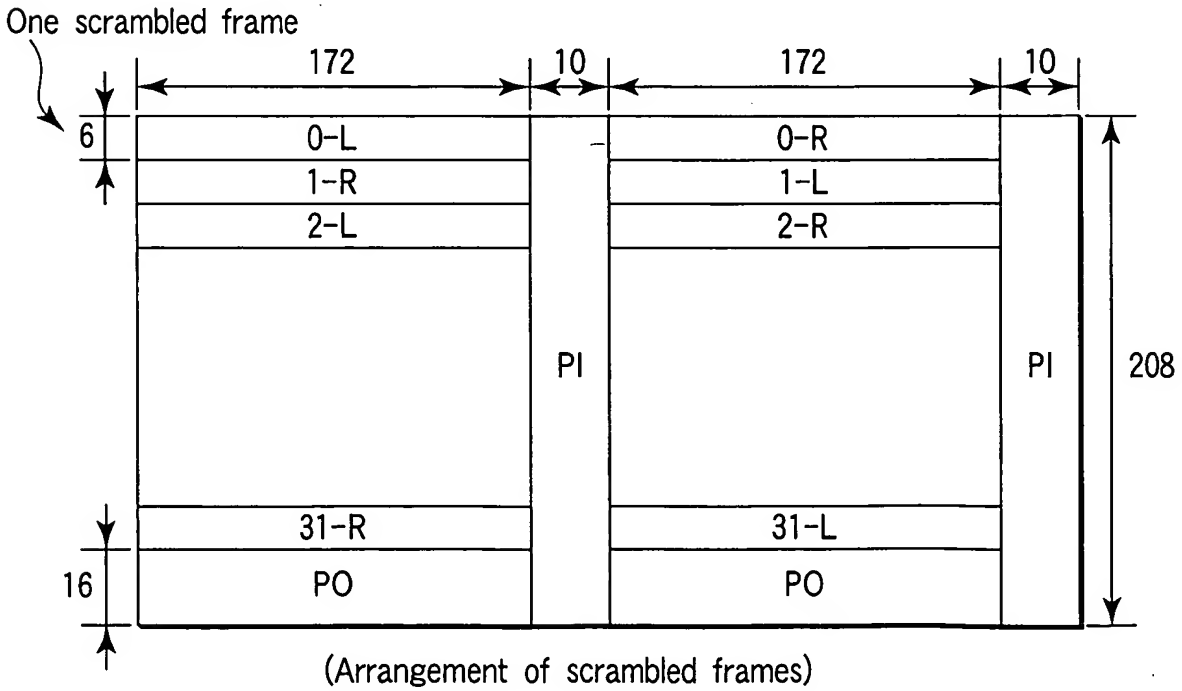


Feedback register



(ECC block structure)

FIG. 21



(Arrangement of scrambled frames)

FIG. 22

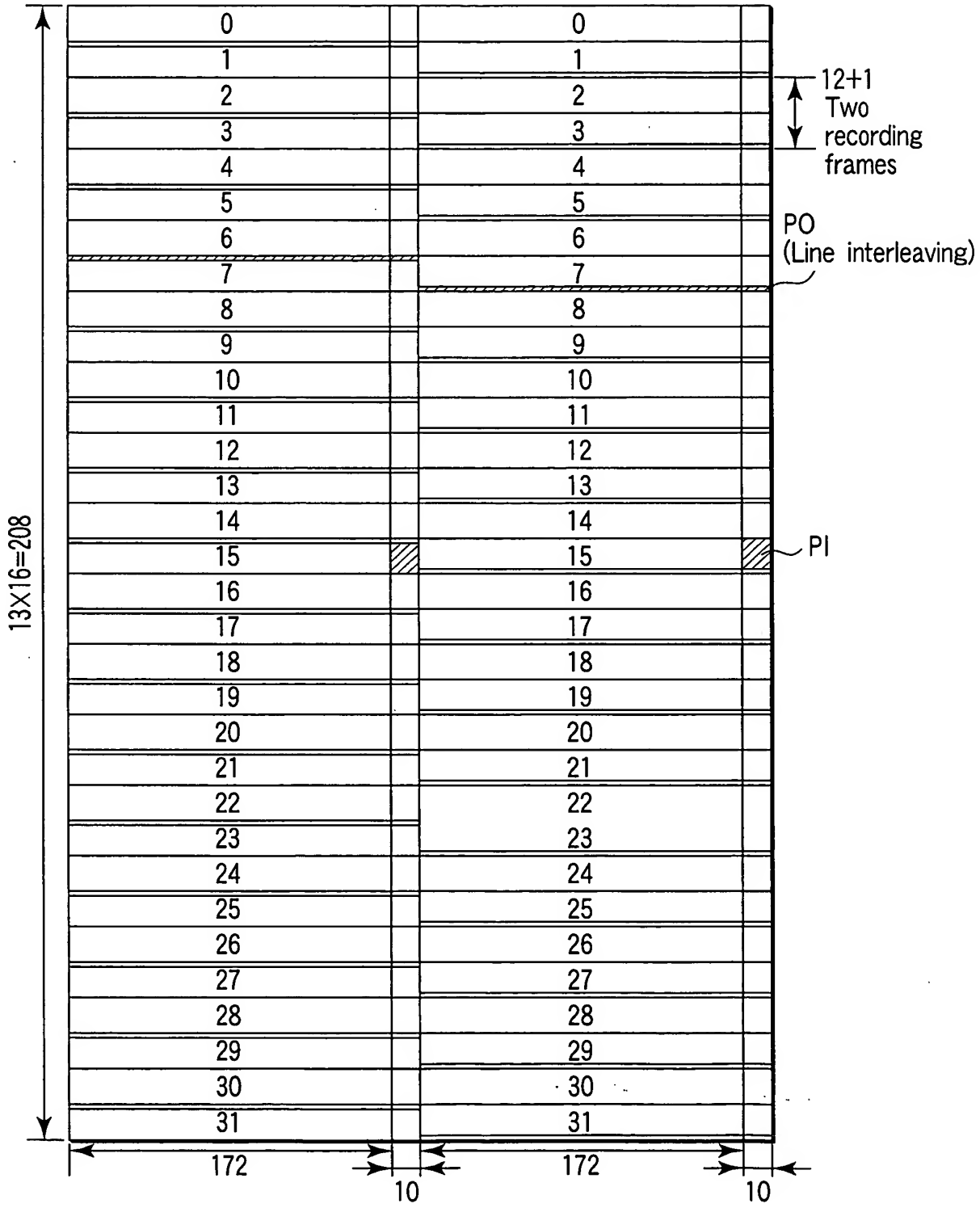

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
13X16=208
12+1
Two
recording
frames
PO
(Line interleaving)
PI
172
10
172
10

FIG. 23

FIG. 24A

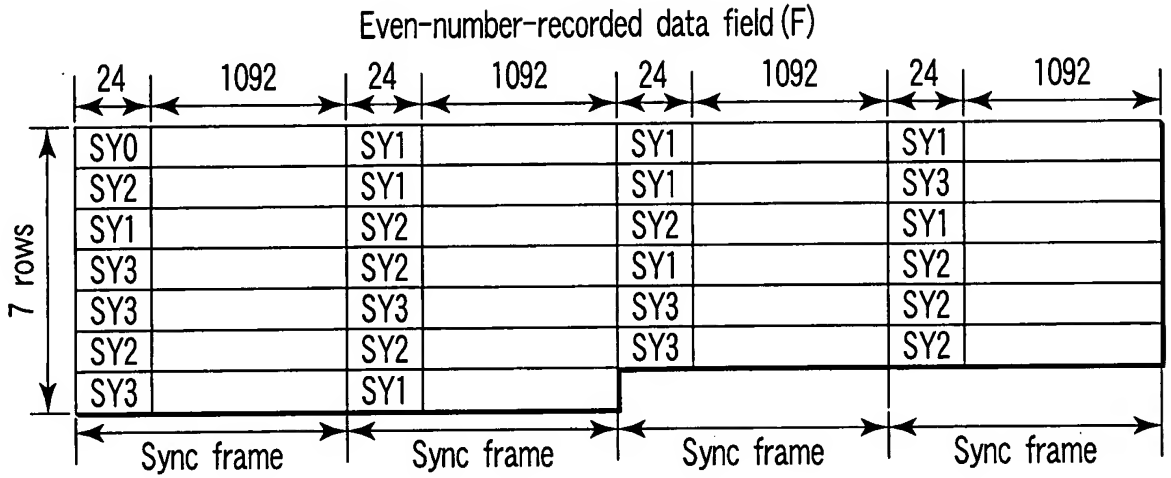


FIG. 24B

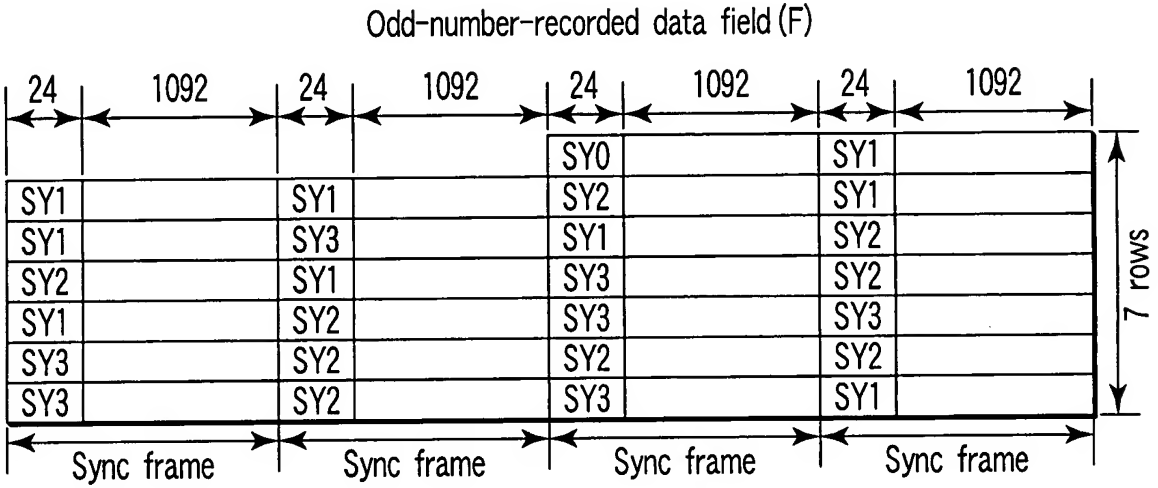


FIG. 25

State0

		(MSB) Primary SYNC codes (LSB)					(MSB) Secondary SYNC codes (LSB)			
SY0	=	000010	101000	000000	001001	/	000010	001000	000000	001001
SY1	=	100001	001000	000000	001001	/	100010	101000	000000	001001
SY2	=	100100	001000	000000	001001	/	101000	101000	000000	001001
SY3	=	101000	001000	000000	001001	/	101010	001000	000000	001001

State1

		(MSB) Primary SYNC codes (LSB)					(MSB) Secondary SYNC codes (LSB)			
SY0	=	000100	101000	000000	001001	/	000100	001000	000000	001001
SY1	=	001001	001000	000000	001001	/	001010	101000	000000	001001
SY2	=	010000	101000	000000	001001	/	010000	001000	000000	001001
SY3	=	010100	001000	000000	001001	/	010101	001000	000000	001001

(SYNC code)

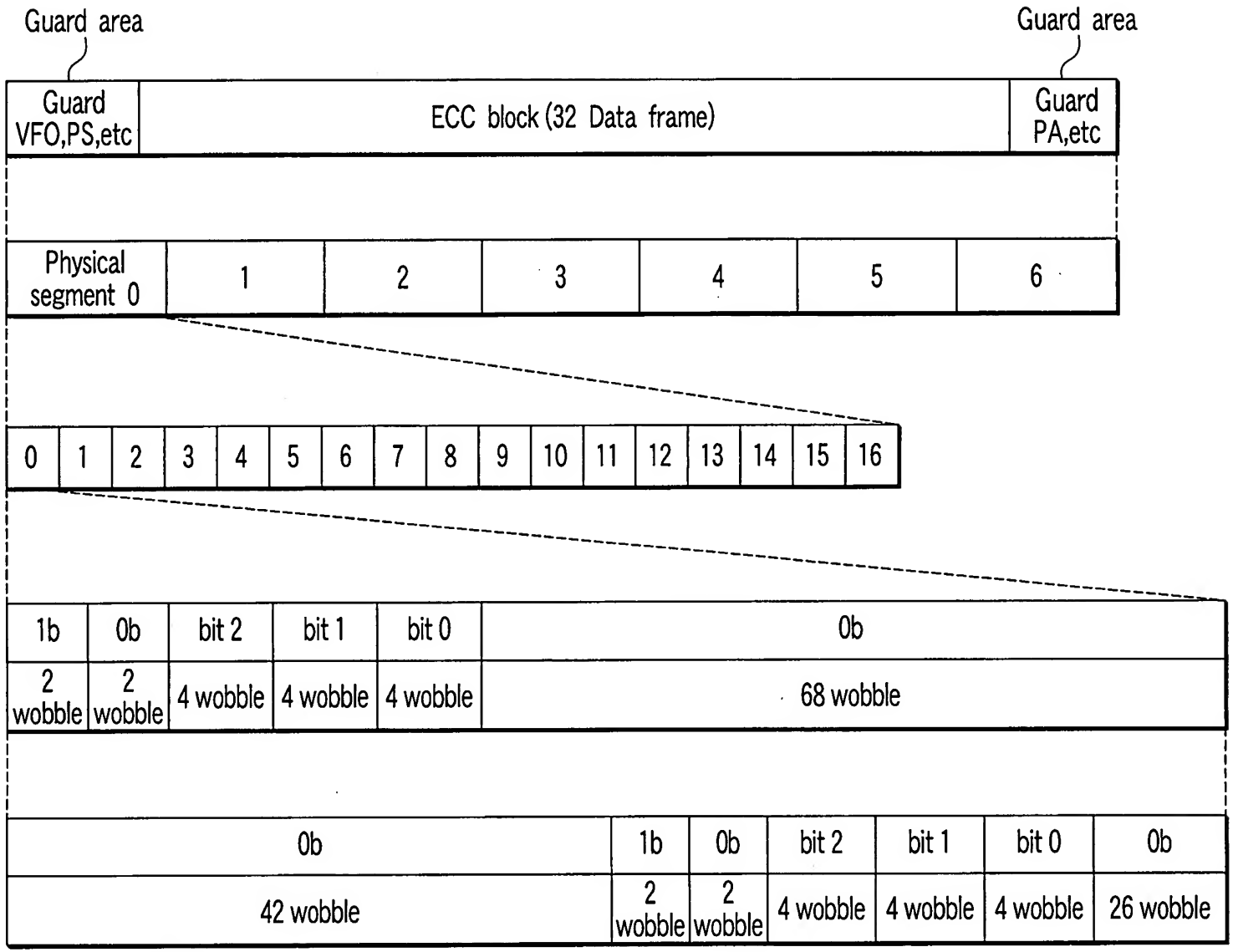


FIG. 26A

FIG. 26B

FIG. 26C

FIG. 26D

FIG. 26E

FIG. 27A

(Primary) (Layout of wobble data unit)

SYNC	1b	0b	1b	0b
	6 wobble	4 wobble	6 wobble	68 wobble

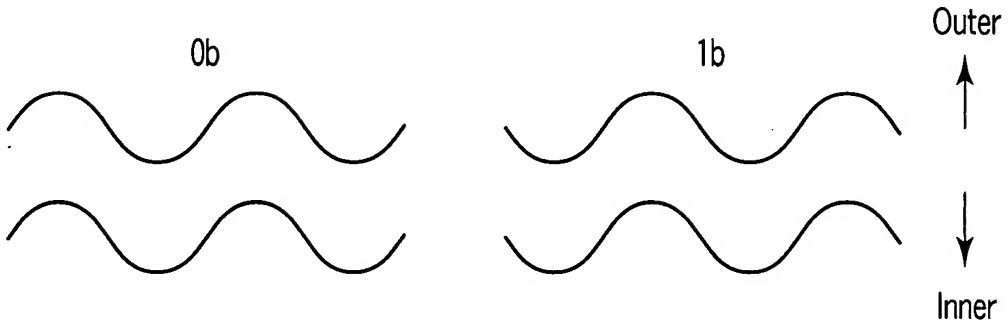
FIG. 27B

Data	1b	0b	bit 2	bit 1	bit 0	0b
	2 wobble		4 wobble	4 wobble	4 wobble	68 wobble

FIG. 27C

monotone	0b
	84 wobble

FIG. 27D



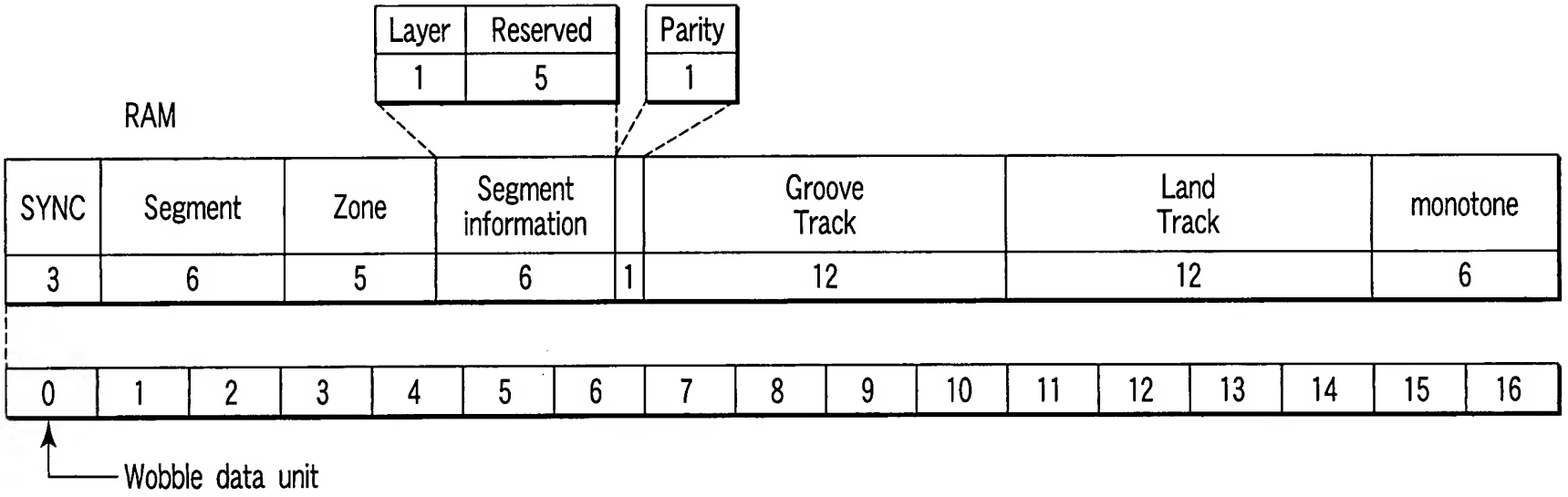


FIG. 28A

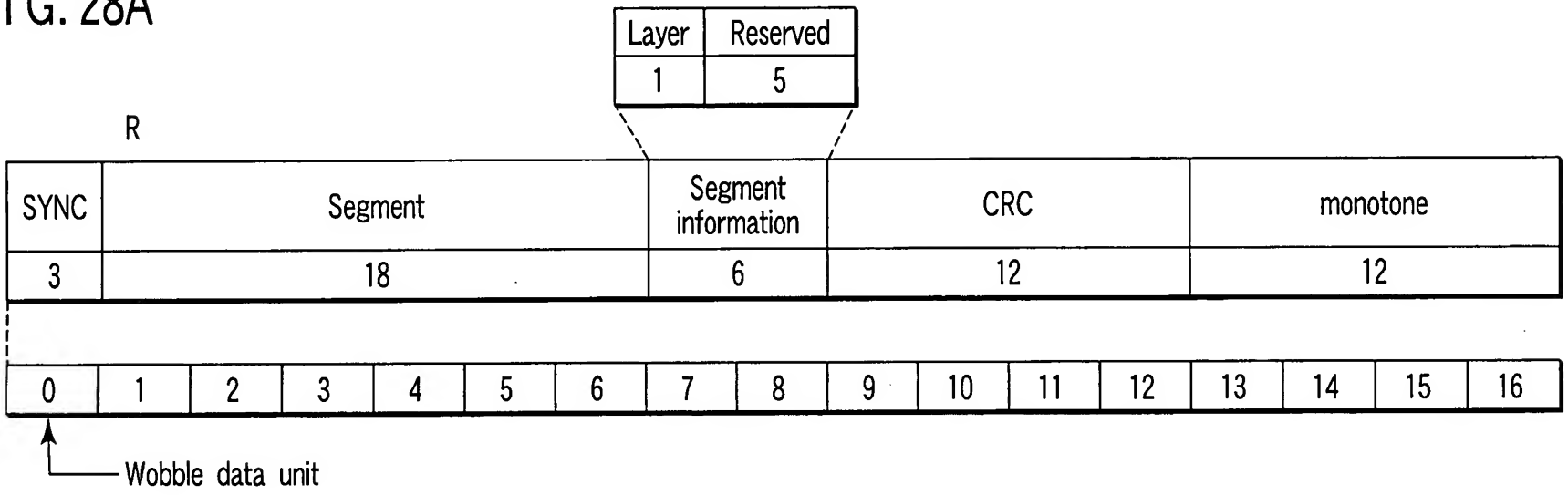


FIG. 28B

Outer edge of disk

↑

Groove	SYNC	Segment	Zone	Segment information	Parity	Groove track (m+2)	-	monotone
Land	SYNC	Segment	Zone	Segment information	Parity	-	Land track (m+2)	monotone
Groove	SYNC	Segment	Zone	Segment information	Parity	Groove track (m+1)	-	monotone
Land	SYNC	Segment	Zone	Segment information	Parity	-	Land track (m+1)	monotone
Groove	SYNC	Segment	Zone	Segment information	Parity	Groove track (m)	-	monotone
Land	SYNC	Segment	Zone	Segment information	Parity	-	Land track (m)	monotone

↓

Inner edge of disk

FIG. 29

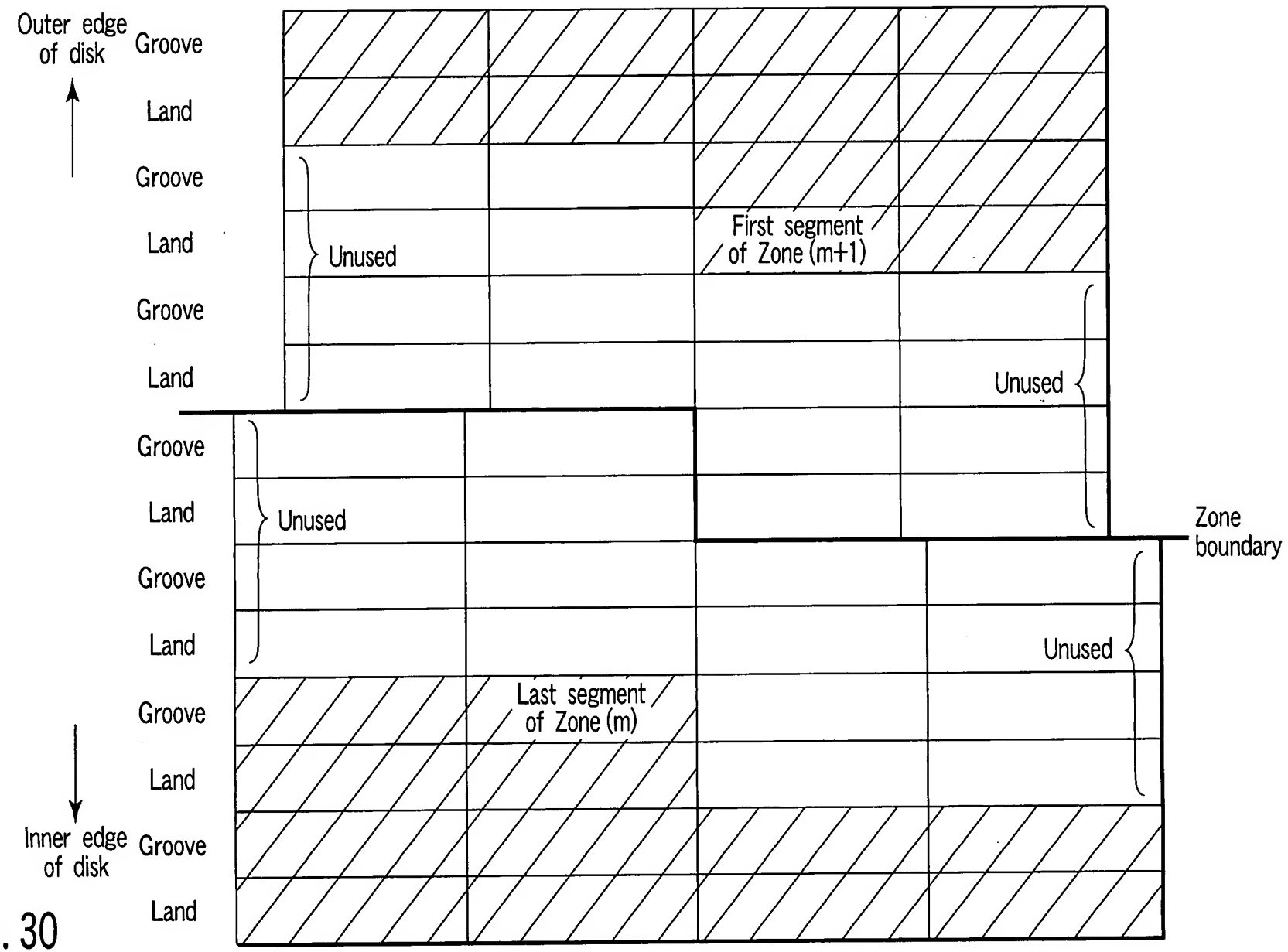
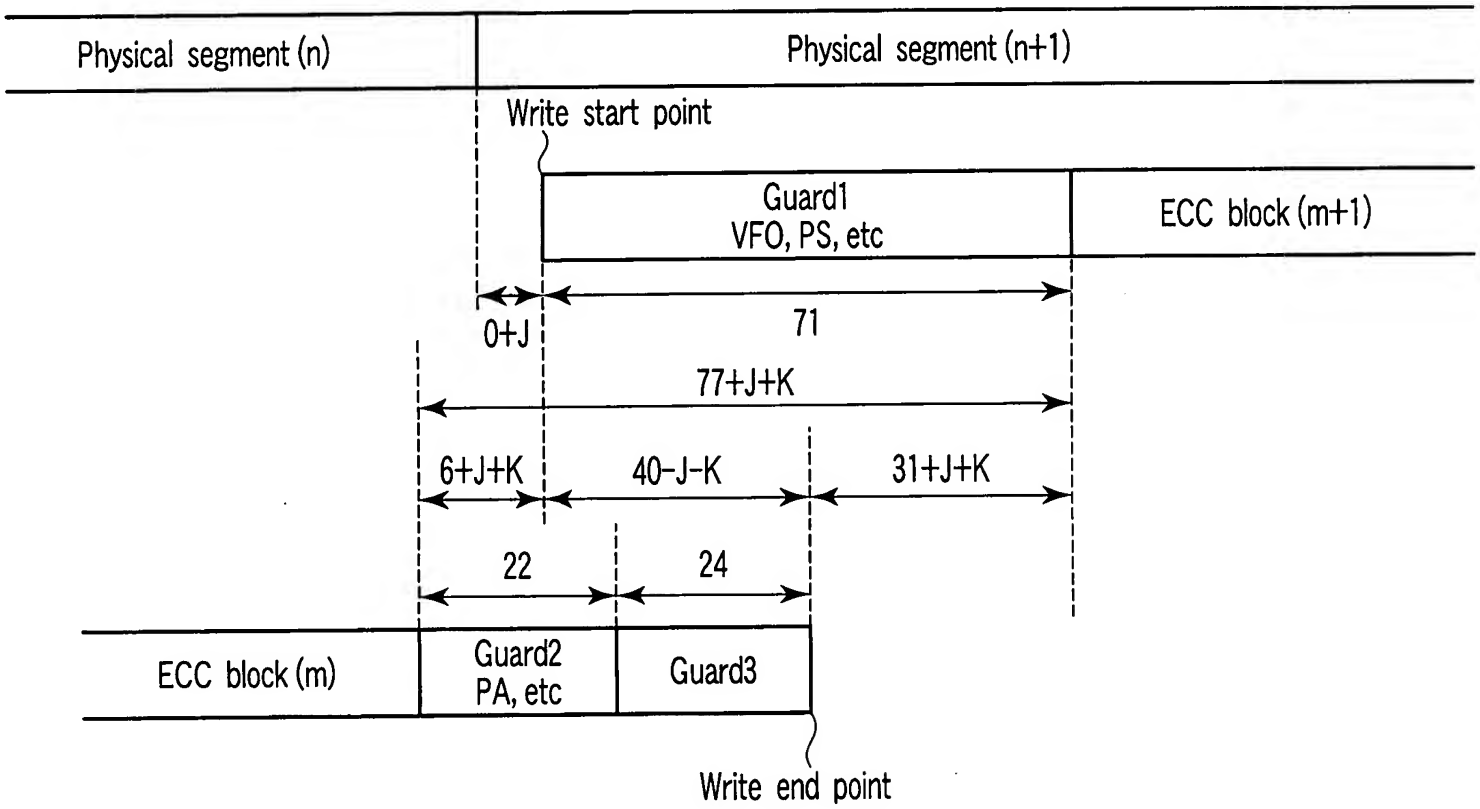

Outer edge of disk
Groove
Land
Groove
Land
Groove
Land
Groove
Land
Groove
Land
Groove
Land
Groove
Land
Inner edge of disk
Groove
Land
Unused
First segment of Zone (m+1)
Unused
Unused
Zone boundary
Unused
Last segment of Zone (m)

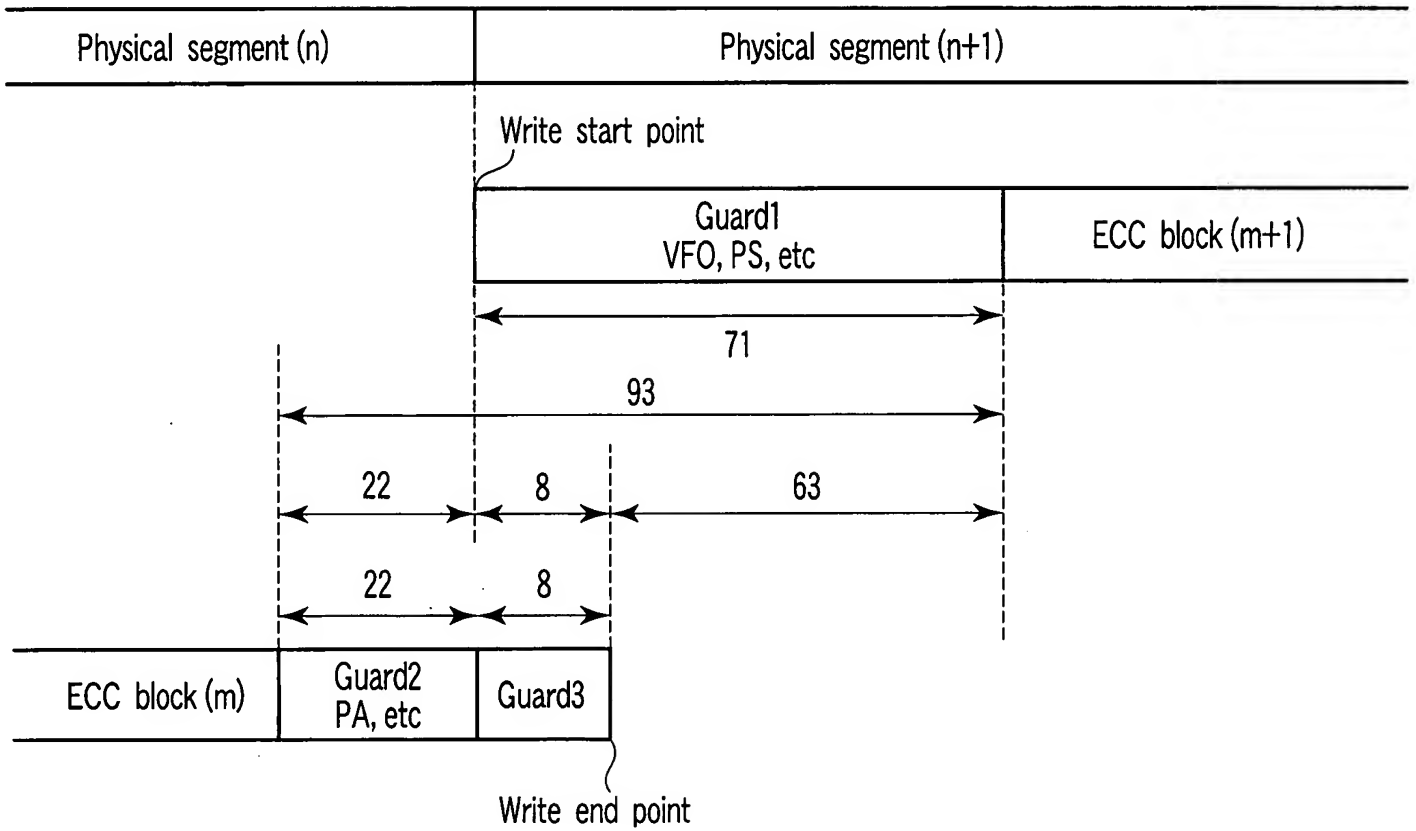
FIG. 30



Random shift
shift value for ECC block (m+1) J=0~15
shift value for ECC block (m) K=0~15

Minimum value of Guard 1 properly reproduced 31Byte
Minimum value of Guard 2 properly reproduced 6Byte
Minimum value of overlap to prevent unrecorded parts from being left 8Byte

FIG. 31



Guard 1 properly reproduced contains 47 bytes
Guard 2 properly reproduced contains 22 bytes
Overlap to prevent unrecorded parts from being left contains 8 bytes

FIG. 32

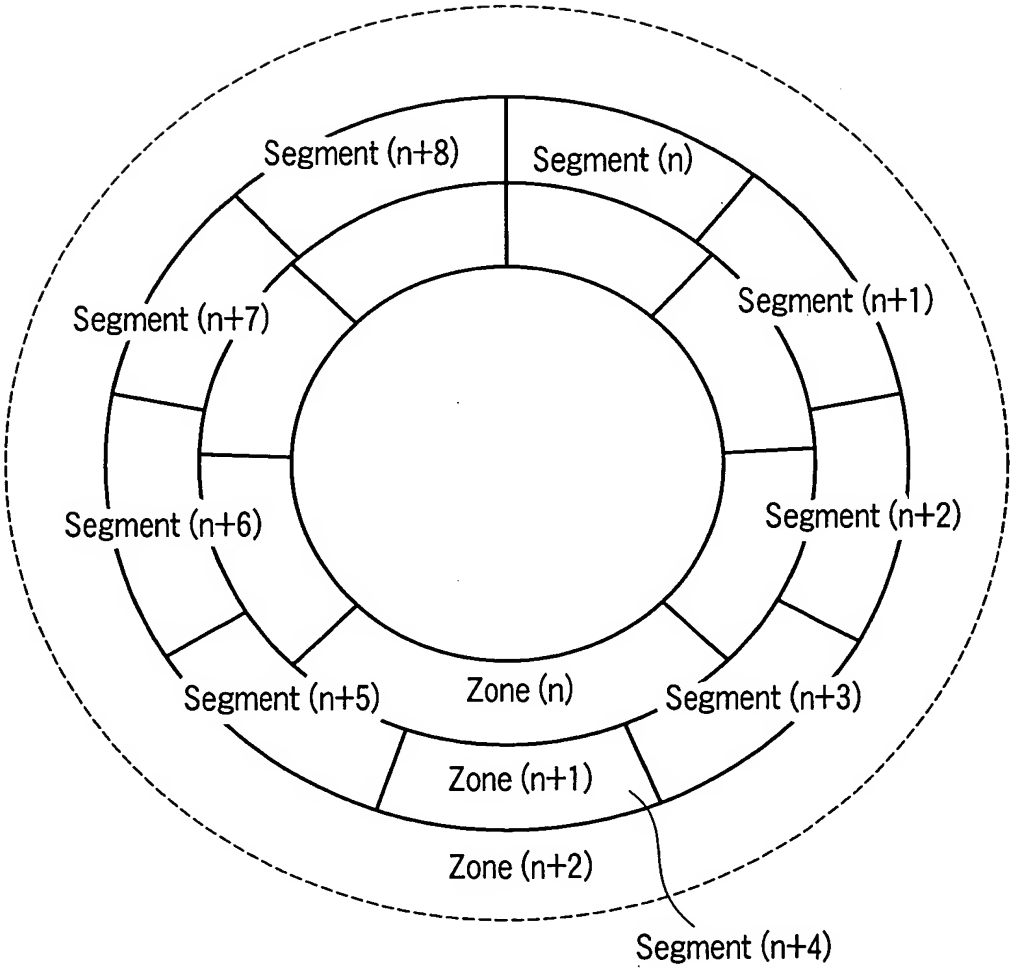
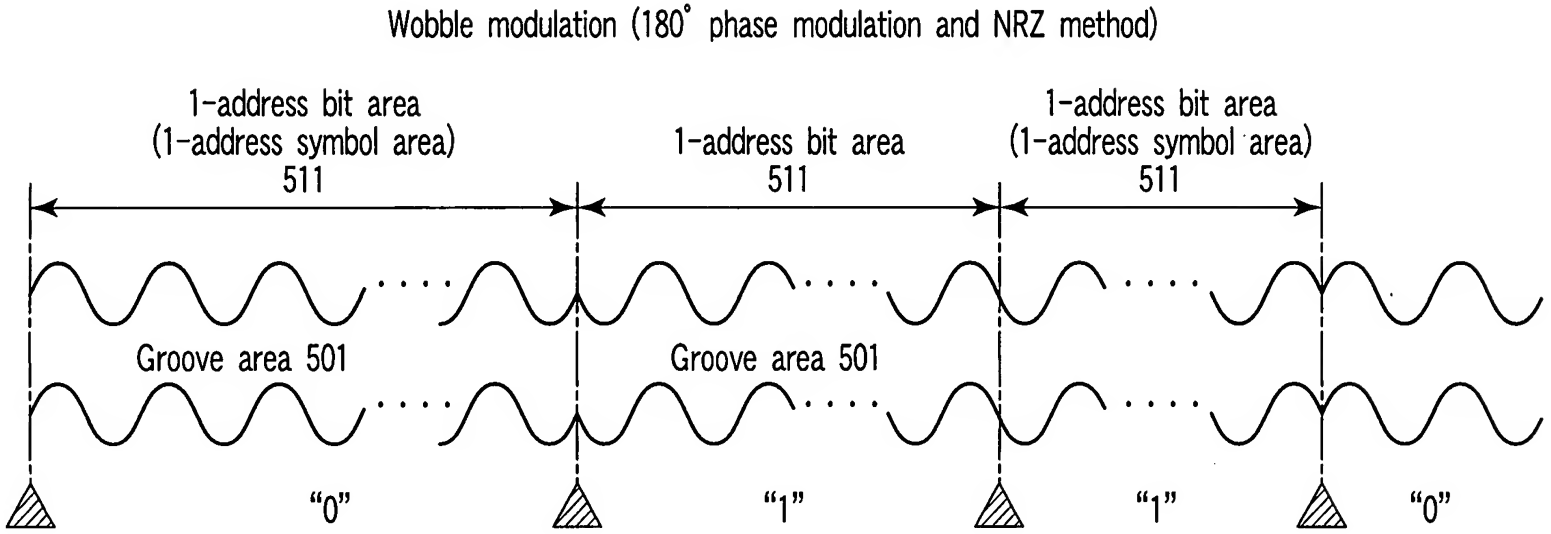

Segment (n+8)
Segment (n)
Segment (n+7)
Segment (n+1)
Segment (n+6)
Segment (n+2)
Segment (n+5)
Zone (n)
Segment (n+3)
Zone (n+1)
Zone (n+2)
Segment (n+4)

FIG. 33



☆ 1-address bit area 511 (expressed in 8 wobbles or 12 wobbles)
☆ Frequency, amplitude, and phase in 1-address bit area = constant everywhere
☆ Boundary part of 1-address bit area 511 (180° or 0° phase shift)

FIG. 34

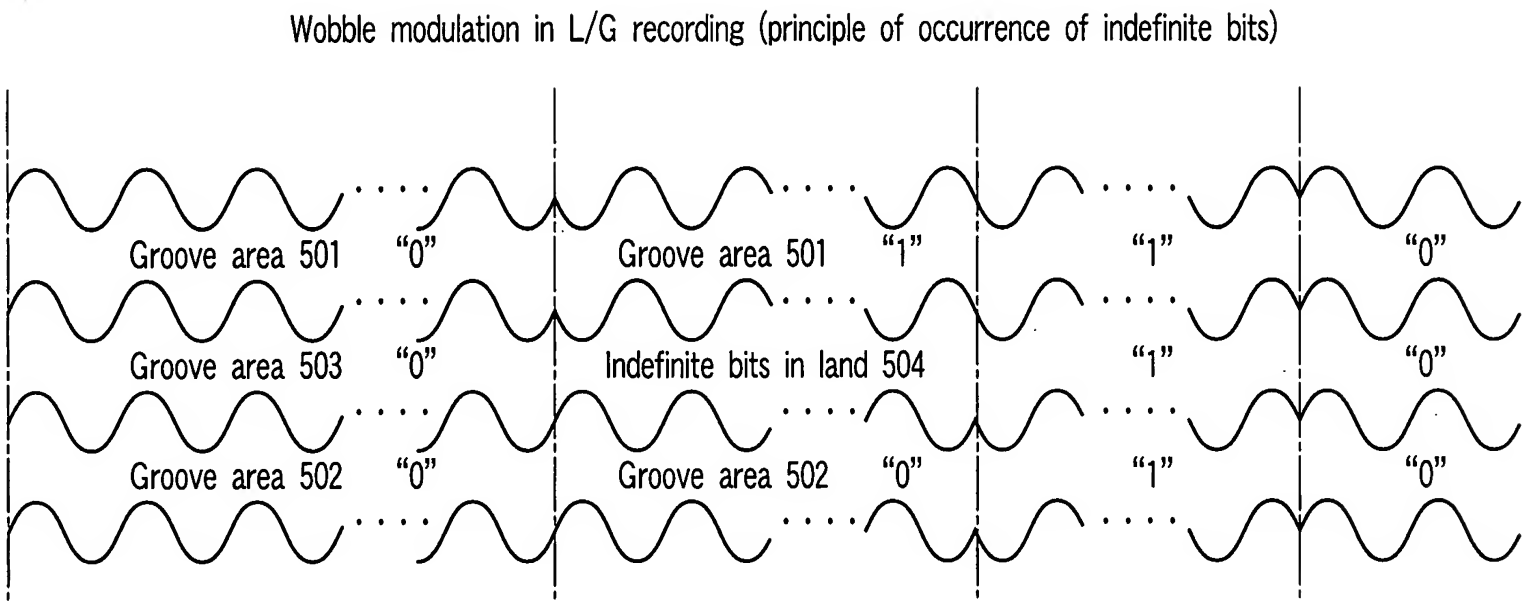

Wobble modulation in L/G recording (principle of occurrence of indefinite bits)
Groove area 501
"0"
Groove area 501
"1"
"1"
"0"
Groove area 503
"0"
Indefinite bits in land 504
"1"
"0"
Groove area 502
"0"
Groove area 502
"0"
"1"
"0"

FIG. 35

Example of Gray code

Decimal number	Conventional binary representation	Gray code representation
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

FIG. 36

(Configuration of information recording and reproducing apparatus) (particularly centering on the recording system)

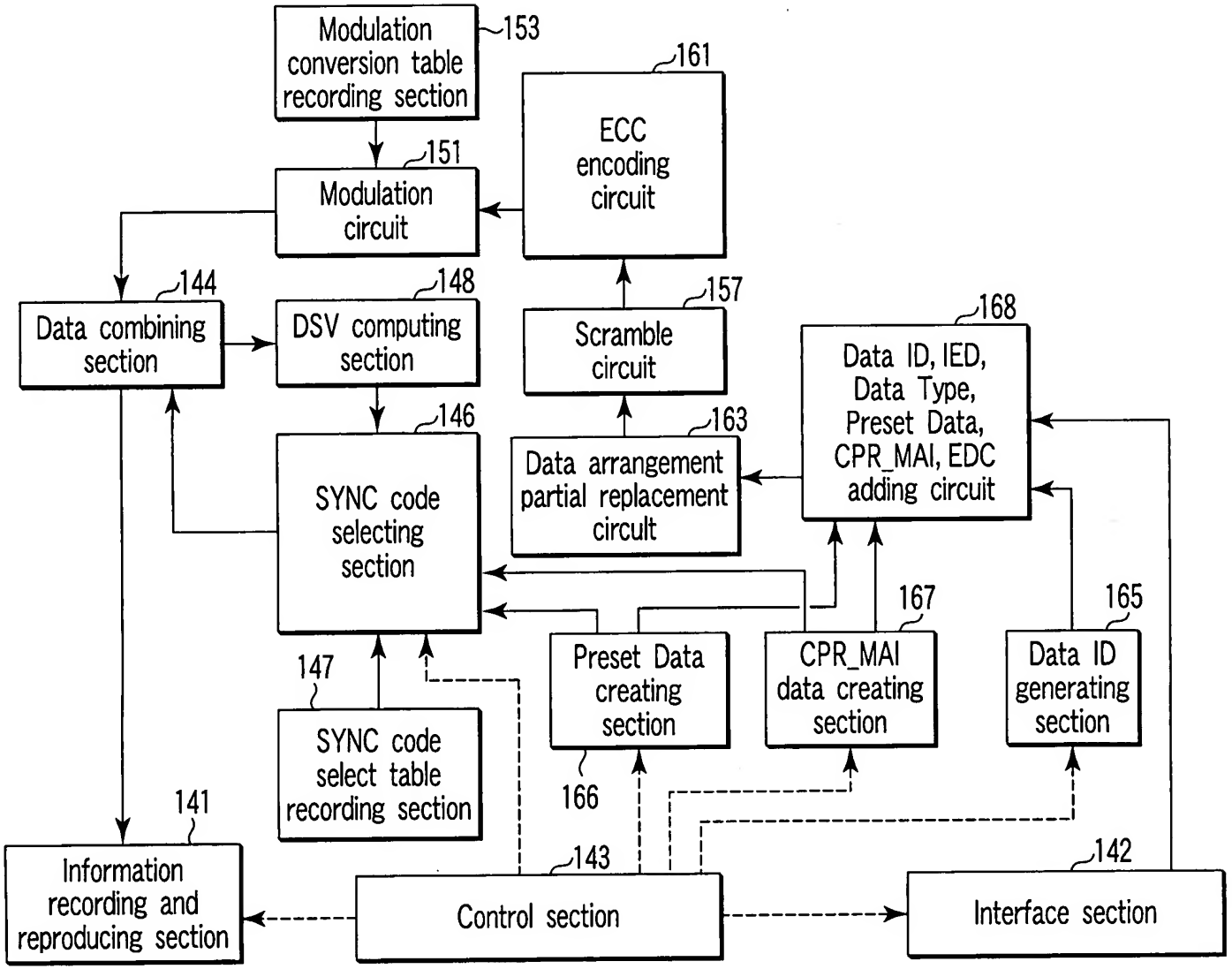


FIG. 37

(Configuration of information recording and reproducing apparatus) (particularly centering on the reproducing system)

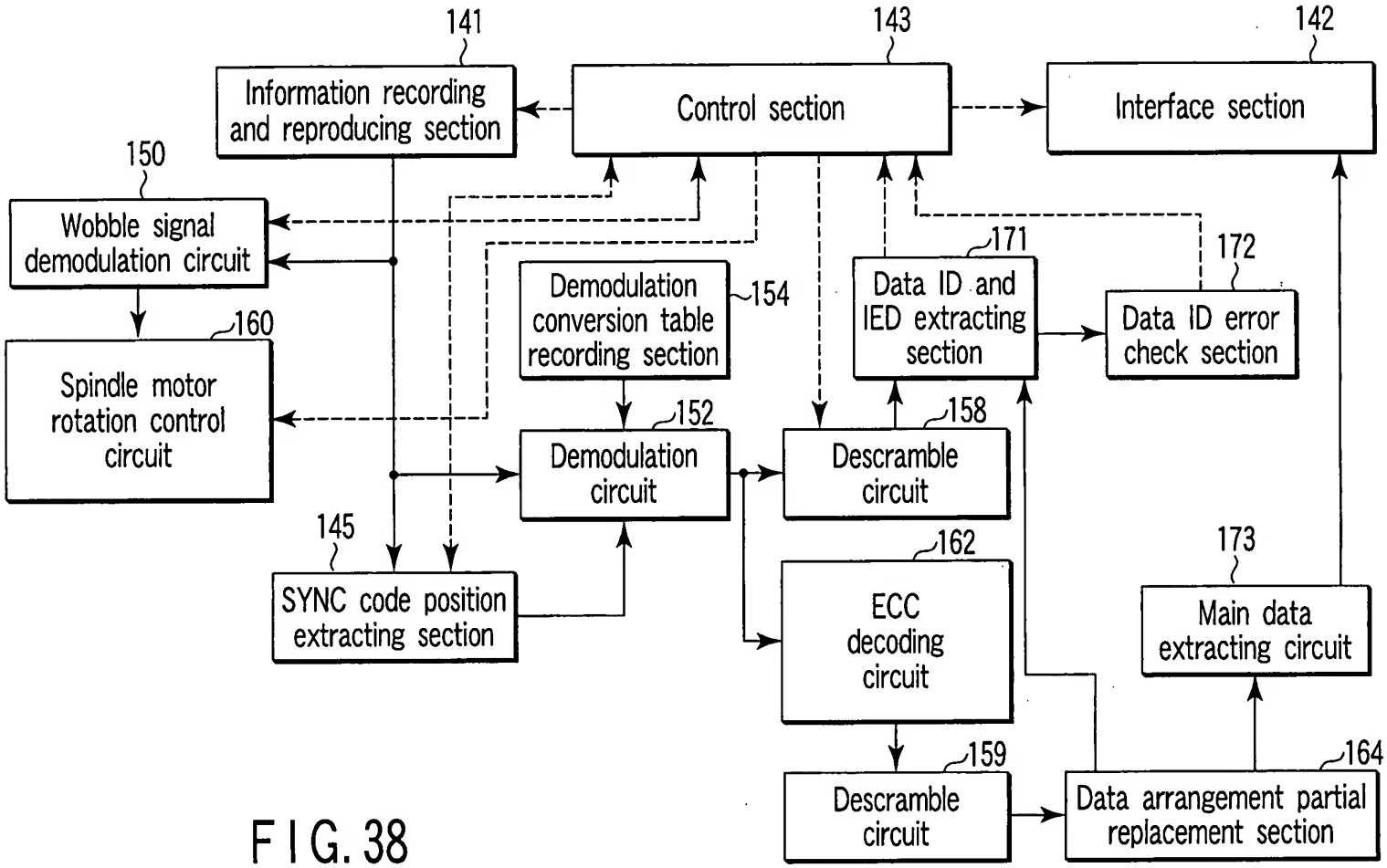


FIG. 38